# **Architecture Considerations for Massively Parallel Hardware Security Platform**

## By Dr P. J. Narayanan

Professor & Director International Institute of Information Technology Gachibowli Hyderabad, INDIA 500 032



**Biography: P. J Narayana** received his B. Tech. (Hons.) degree from Indian Institute of Technology, Kharagpur, India, in 1984, the M.S. degree from the University of Maryland, College Park, USA in 1989, and the Ph.D. degree from University of Maryland, College Park, USA – 1992, all in Computer Science. Since June 2013 he is the Director of IIT Hyderabad From 1984 to 1986 he was an Associate Development Engineer in the CMC R&D, Secunderabad, India, and from 1986 to 1992 he was Graduate Assistant in the Department of Computer Science, University of Maryland. From 1992 to 1996 he was Research Faculty Member in Robotics Institute, Carnegie Mellon University, Pittsburgh. From 1996 to 2000 he was Scientist D, E and Head of Computer Vision & Virtual RealityCentre for Artificial Intelligence & Robotics, DRDO, Bangalore. From 2000 to 2013 he was Head, Centre for Visual Information Technology in International Institute of Information Technology, Hyderabad.an Associate Professor at the same place from 1984 to 1987. From 1987 to May 2009. From July 2013 he was the Director of International Institute of Information Technology, Hyderabad.

His research interest is in Computer Vision, Computer Graphics and Parallel Computing. He is also interested in Virtual reality, computational displays. Professor Narayana is a Steering Committee Member, NRDMS, Department of Science and Technology, 2013 onwards. He was Project Advisory & Monitoring Committee in Department of Science and Technology, 2008-2011. He was NMITLI Project Monitoring Committee, CSIR, 2008 onwards. He was Euro-India SPIRIT Working Group Member, 2010-2012. He was Working Group member of TDIL, Ministry of Communication & Information Technology, 2010-2012

#### **Awards and Honours**

- ACM Presidential Award. 2013.
- Best paper. Eurographics Symposium on Parallel Graphics and Visualization. 2010.
- CUDA Fellow in recognition of contributions to GPGPU by Nvidia Corporation. 2008
- Best applications paper. International Conference on Multisensor Fusion and Integration. 1996.
- Captain, University of Maryland programming team. Honourable mention in the world finals. 1989.
- Fifth rank in the state of Kerala in secondary school board examinations. 1978.

### **Program Committee Member or Reviewer:**

- ICCV 2005, 2009; CVPR 2008, 2009, 2010, 2011; ECCV 2004, 2006, 2008, 2010.
- ICPR 2008, 2010, 2012; ICVGIP 2000-2012; WACV 2006.
- Eurographics 2011; EuroVis 2009; ACM Multimedia Modelling 2008.
- SIGGRAPH Asia/ACM ToG. 2009, 2011.
- HiPC 2004, 2008; LCA-GPGPU 2010.

## General Chair:

Indian Conference on Computer Vision, Graphics, and Image Processing (ICVGIP). 2000.

#### Journal Reviewer:

- International Journal on Computer Vision (IJCV).
- IEEE Transactions on Pattern Analysis and Machine Intelligence (PAMI).
- IEEE Journal of Mathematical Imaging and Vision.
- IEEE Transactions on Circuits and Systems for Video Technology (CSVT).
- IEEE Transactions on Visualization and Computer Graphics (TVCG).
- IEEE Transactions on Parallel and Distributed Systems (TPDS).
- IEEE Transactions on Very Large Scale Integration (TVLSI).
- Journal of Parallel and Distributed Computing (JPDC).
- The Visual Computer (TVC).